

IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

- 1 1. (Original) A method for routing data within a host device comprising:
2 receiving a data block at a receiver of the host device;
3 storing the data block in a receiver buffer;
4 determining an input virtual channel corresponding to the data block;
5 updating an input virtual channel linked list corresponding to the input virtual channel to include
6 the data block;
7 determining an output virtual channel for the data block;
8 transferring the data block from the input virtual channel linked list of the receiver buffer to a
9 destination within the host device via the output virtual channel; and
10 updating the input virtual channel linked list to remove the data block.
- 1 2. (Original) The method of claim 1, wherein determining an output virtual channel for the data
2 block includes processing one or more of the input virtual channel, a header corresponding to the data
3 block, a protocol corresponding to the data block, source identifier/address corresponding to the data
4 block, and a destination identifier/address corresponding to the data block.
- 1 3. (Original) The method of claim 1, wherein:
2 storing the data block in the receiver buffer includes storing the data block in the receiver buffer
3 at an old free linked list head address; and
4 updating an input virtual channel linked list corresponding to the input virtual channel to include
5 the data block comprises:
6 reading a new free linked list head address from the receiver buffer at an old free linked list head
7 address;
8 writing the new free linked list head address to a free linked list head register;
9 writing the old free linked list head address to the receiver buffer at the old input virtual channel
10 linked list tail address; and
11 writing the old free linked list head address to an input virtual channel linked list tail register.

1 4. (Original) The method of claim 1, wherein:
2 transferring the data block from the input virtual channel linked list of the receiver buffer to a
3 destination within the host device via the output virtual channel includes reading the data block from the
4 receiver buffer at an old input virtual channel linked list head address; and
5 updating the input virtual channel linked list to remove the data block comprises:
6 reading a new input virtual channel linked list head address from the receiver buffer at
7 the old input virtual channel linked list head address;
8 writing the new input virtual channel linked list head address to an input virtual channel
9 linked list head register;
10 writing the old input virtual channel linked list head address to the receiver buffer at an
11 old free linked list tail address; and
12 writing the old input virtual channel linked list head address to a free linked list tail
13 register.

1 5. (Original) The method of claim 1, further comprising writing a data block to the receiver buffer
2 and reading a data block from the receiver buffer in a single read/write cycle.

1 6. (Original) The method of claim 1, further comprising anticipating the write of a data block to the
2 receiver buffer in a subsequent read/write cycle by reading a new free linked list head address from the
3 receiver buffer at an old free linked list head address in a current read/write cycle.

1 7. (Original) The method of claim 1, further comprising in a common read/write cycle in which a
2 first data block is read from the receiver buffer and a second data block is written to the receiver buffer:
3 reading the first data block and a new input virtual channel head address from the receiver buffer
4 at an old input virtual channel head address;
5 writing the new input virtual channel head address to the input virtual channel head register;
6 writing the second data block to the receiver buffer at the old input virtual channel head address;
7 writing the old input virtual channel head address to an input virtual channel tail register; and
8 writing the old input virtual channel head address to the receiver buffer at an old input virtual
9 channel tail address.

1 8. (Original) The method of claim 1, further comprising supporting a plurality of input virtual
2 channel linked lists, wherein each input virtual channel linked list corresponds to a respective input virtual
3 channel.

1 9. (Original) The method of claim 1, further comprising supporting a free linked list that includes a
2 plurality of vacant data blocks of the receiver buffer.

1 10. (Original) The method of claim 1, further comprising maintaining a mapping indicating a
2 relationship between a plurality of input virtual channels and a plurality of output virtual channels.

1 11. (Original) A method for routing data within a host device comprising:
2 receiving a data block at a receiver of the host device, the data block received via an input virtual
3 channel;
4 storing the data block in a receiver buffer;
5 when the input virtual channel has identified therewith an output virtual channel updating an
6 output virtual channel linked list corresponding to the output virtual channel to include the data block; and
7 when the input virtual channel has not identified therewith an output virtual channel:
8 updating an input virtual channel linked list corresponding to the input virtual channel to include
9 the data block;
10 processing the data block to determine an output virtual channel for the data block;
11 updating an output virtual channel linked list corresponding to the output virtual channel to
12 include the data block; and
13 updating the input virtual channel linked list to remove the data block.

1 12. (Currently Amended) The method of ~~claim 12~~ claim 11, further comprising:
2 transferring the data block from the receiver buffer to a destination within the host device based
3 upon a corresponding output virtual channel; and
4 updating the output virtual channel linked list to remove the data block.

1 13. (Original) The method of claim 11, wherein:
2 storing the data block in the receiver buffer includes storing the data block in the receiver buffer
3 at an old free linked list head address; and
4 updating an input virtual channel linked list corresponding to the input virtual channel to include
5 the data block comprises:
6 reading a new free linked list head address from the receiver buffer at an old free linked list head
7 address;
8 writing the new free linked list head address to a free linked list head register;
9 writing the old free linked list head address to the receiver buffer at the old input virtual channel
10 linked list tail address; and
11 writing the old free linked list head address to an input virtual channel linked list tail register.

1 14. (Original) The method of claim 11, further comprising writing a data block to the receiver buffer
2 and reading a data block from the receiver buffer in a single read/write cycle.

1 15. (Original) The method of claim 11, further comprising anticipating the write of a data block to the
2 receiver buffer in a subsequent read/write cycle by reading a new free linked list head address from the
3 receiver buffer at an old free linked list head address in a current read/write cycle.

1 16. (Original) The method of claim 11, further comprising in a common read/write cycle in which a
2 first data block is read from the receiver buffer and a second data block is written to the receiver buffer:
3 reading the first data block and a new output virtual channel head address from the receiver buffer
4 at the old output virtual channel head address;
5 writing the new output virtual channel head address to the output virtual channel head register;
6 writing the second data block to the receiver buffer at the old output virtual channel head address;
7 writing the old output virtual channel head address to an output virtual channel tail register; and
8 writing the old output virtual channel head address to the receiver buffer at the old output virtual
9 channel head address.

1 17. (Original) The method of claim 11, further comprising supporting a plurality of input virtual
2 channel linked lists, wherein each input virtual channel linked list corresponds to a respective input virtual
3 channel.

1 18. (Original) The method of claim 11, further comprising supporting a plurality of output virtual
2 channel linked lists, wherein each output virtual channel linked list corresponds to a respective output
3 virtual channel.

1 19. (Original) The method of claim 11, further comprising supporting a free linked list that includes a
2 plurality of vacant data blocks of the input buffer.

1 20. (Original) A received data processing and storage system comprising:
2 an input that receives data blocks corresponding to a plurality of input virtual channels;
3 a routing module that determines an output virtual channel for data blocks based upon their
4 respective input virtual channels;
5 a receiver buffer operable to instantiate an input virtual channel linked list for storing data blocks
6 on an input virtual channel basis and to instantiate a free list that identifies free data locations;
7 a linked list control module operably coupled to the receiver buffer;
8 input virtual channel linked list registers operably coupled to the linked list control module; and
9 free linked list registers operably coupled to the linked list control module.

1 21. (Original) The received data processing and storage system of claim 20, further comprising an
2 output that transmits data blocks corresponding to a plurality of input virtual channels.

1 22. (Original) The received data processing and storage system of claim 20, wherein:
2 the receiver buffer is further operable to instantiate an output virtual channel linked list for storing
3 data blocks on an output virtual channel basis; and
4 the system further comprises output virtual channel linked list registers operably coupled to the
5 linked list control module and an input virtual channel to output virtual channel map.

1 23. (Original) The received data processing and storage system of claim 20, wherein the receiver
2 buffer comprises:
3 a pointer memory; and
4 a data memory, wherein a single address addresses corresponding locations of the pointer
5 memory and of the data memory.

1 24. (Original) The received data processing and storage system of claim 23, wherein the receiver
2 buffer further comprises a packet status memory, wherein a single address addresses corresponding
3 locations of the pointer memory, the data memory, and the packet status memory.

1 25. (Original) The received data processing and storage system of claim 23, further comprising a
2 pointer memory read port, a pointer memory write port, a data memory read port, and a data memory
3 write port, each of which can access the receiver buffer in a common read/write cycle.

1 26. (Original) The received data processing and storage system of claim 25, wherein:
2 a single pointer memory location can be read from and written to in a common read/write cycle;
3 and
4 a single data memory location can be read from and written to in a common read/write cycle.

1 27. (Original) The received data processing and storage system of claim 20, wherein the receiver
2 buffer comprises:
3 a pointer memory;
4 a data memory;
5 a packet status memory; and
6 wherein a single address addresses corresponding locations of the pointer memory, the data
7 memory, and the packet status memory.

1 28. (Original) The received data processing and storage system of claim 27, further comprising:
2 a pointer memory read port;
3 a pointer memory write port;
4 a data memory read port;
5 a data memory write port;
6 a packet status memory read port; and
7 a packet status memory write port.

1 29. (Original) The received data processing and storage system of claim 28, wherein:
2 a single pointer memory location can be read from and written to in a common read/write cycle;
3 a single data memory location can be read from and written to in a common read/write cycle; and
4 a single packet status memory location can be read from and written to in a common read/write
5 cycle.